IN THE CLAIMS

1-24. (Canceled)

25. (Previously Presented) A system comprising:

memory including one or more memory cells;

a memory controller;

an operating system configured to dynamically allocate and de-allocate the memory and to identify allocated and de-allocated memory to the memory controller based on whether or not virtual-to-physical memory mapping portions are active; and

recent-access flags associated with the one or more memory cells, the recent-access flags being configurable to indicate whether corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the system is configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval;

wherein the memory controller is responsive to the operating system to operate non-allocated memory at reduced power.

26. (Original) A system as recited in claim 25, wherein the memory is dynamically refreshable memory and the memory controller operates the non-allocated memory at reduced power by omitting refreshing of non-allocated memory.

27. (Canceled)

28. (Previously Presented) A system as recited in claim 25, wherein the memory controller is configured to cache at least some of the allocated memory and to omit refreshing of the cached memory.

29. (Previously Presented) A system as recited in claim 25, further comprising:

a plurality of use bits corresponding respectively to memory rows, wherein each use bit is configurable to indicate whether its corresponding memory row is currently allocated.

30. (Original) A system as recited in claim 25, further comprising a plurality of use bits on the memory controller corresponding respectively to memory rows, wherein each use bit is configurable to indicate whether its corresponding memory row is currently allocated, and wherein the memory controller is configured to omit refreshing of memory rows that are not currently allocated.

31. (Previously Presented) A system as recited in claim 25, wherein the memory comprises a

plurality of discrete memory devices, the system further comprising a plurality of use bits on the memory devices corresponding respectively to memory rows, wherein each use bit is configurable to indicate whether its corresponding memory row is currently allocated, and wherein the memory controller is configured to omit refreshing of memory rows that are not currently allocated by configuring the use bits.

32. (Previously Presented) In a system having dynamically refreshable memory rows, a method of memory power management, comprising:

indicating that memory rows, upon being transferred to a cache, are not in use prior to when the transferred memory rows are written-to in the cache;

keeping track of which memory rows are in use and therefore need refreshing;

periodically refreshing those memory rows that are in use; and

omitting refreshing of memory rows that are not in use.

33. (Previously Presented) A method as recited in claim 32, further comprising:

determining which rows have been accessed in a manner that refreshed the memory rows during a previous refresh cycle interval, wherein the determining act is performed by utilizing a plurality of recent-access flags associated with each of the memory rows; and

omitting refreshing of memory rows that have been accessed in a manner that refreshed the memory rows during the previous refresh cycle.

34. (Previously Presented) A method as recited in claim 32, wherein the indicating comprises resetting one or more use registers corresponding to the memory rows that have been transferred to the cache.

35. (Original) A method as recited in claim 32, wherein keeping track comprises maintaining a plurality of flags corresponding respectively to the memory rows.

36-51. Canceled

52. (Previously Presented) A method for a memory device comprising:

receiving at the memory device memory allocation and de-allocation notifications from an operating system;

periodically refreshing memory cells that are allocated;

omitting refreshing of memory cells that are de-allocated;

keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval; and

omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle,

wherein the memory allocation and de-allocation notifications are based on virtual memory mapping portions.

53. (Previously Presented) A method as recited in claim 52, further comprising:

responsive to the receiving, setting and unsetting use registers corresponding to memory addresses of the memory allocation and de-allocation notifications, respectively.

54. (Canceled)

55. (Previously Presented) A system as recited in claim 25, wherein the recent-access flags are located on the memory controller, and the memory controller is configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval.

56. (Previously Presented) A system as recited in claim 29, wherein the use bits are implemented as part of the memory cells or as part of the memory controller.

57. (Previously Presented) A method as recited in claim 34, further comprising:

flushing contents of the cache back to the memory rows; and

setting the one or more use registers corresponding to the memory rows to indicate that the memory rows are in use.

58. (Canceled)

59. (Previously Presented) A method as recited in claim 53, wherein the setting and unsetting comprises setting and unsetting use registers that are implemented as part of a memory controller.

60. (Previously Presented) A method as recited in claim 52, wherein the memory device comprises at least one of (i) a memory controller device or (ii) a device having memory cells.

61. (Previously Presented) A memory device that is capable of receiving memory de-allocation notifications from an operating system; the memory device adapted omit refreshing of memory cells of memory portions that have been de-allocated responsive to the memory de-allocation notifications.

62. (Previously Presented) The memory device of claim 61, wherein the memory device comprises at least one of (i) a memory controller device or (ii) a device having the memory cells.

63. (Previously Presented) A memory device as recited in claim 61, wherein the memory device is further capable of receiving memory allocation notifications from the operating system; the memory device further adapted to periodically refresh memory cells of memory portions that have been allocated responsive to the memory allocation notifications.

64 (Previously Presented) A memory device as recited in claim 61, wherein the memory de-allocation notifications are based on virtual memory mapping portions.

65. (Previously Presented) A method for a memory device comprising:

receiving at the memory device memory allocation and de-allocation notifications from an application;

periodically refreshing memory cells that are allocated based on the memory allocation notifications; and

omitting refreshing of memory cells that are de-allocated based on the memory de-allocation notifications.

66. (Previously Presented) A method as recited in claim 65, wherein the memory device comprises at least one of (i) a memory controller device or (ii) a device having the memory cells.

67. (Currently Amended) A method as recited in claim 65, further comprising:

keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval; and

omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval.